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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,551	05/13/2004	Yao-Jen Liang	MTKP0118USA	3550

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EXAMINER	
VIDWAN, JASJIT S	

ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
12/31/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/709,551	LIANG ET AL.	
	Examiner	Art Unit	
	Jasjit S. Vidwan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/08/2007 have been fully considered but they are not persuasive. Applicant argues that Examiner's provided motivation to combine AAPA with Fujii is not sufficient and lacks inventive process that would allow one of ordinary skill in the art to combine the two teachings.

2. With respect to above argument, Examiner disagrees. It should be noted that Fujii teaches all the inventive steps of Applicant's method of transmitting data in a multi-chip system. The only element that Fujii fails to teach is the function of slave chip which is engaged in executing servo control or signal detection. Though Fujii does not teach a system wherein the multi-chip system deals with servo control, it would be obvious to one of ordinary skill in the art to use a cost effective data transmitting method of Fujii in an alternative multi-chip system of servo control as taught by AAPA. Additionally it should be noted that the limitation of servo control is only present in the preamble and thus does not need to be given patentable weight. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). Despite the above reasoning, Examiner provided an acceptable motivation for one to transport the method of transmitting data as provided by Fujii in a system of servo control as well. In light of above arguments, Examiner submits that prior art of record still reads on claimed invention.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3-12 and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art ("Description of the Prior Art") **[herein after AAPA]** and further in view of Fujii, U.S. Patent No: 5,898,695 **[herein after Fujii]**.

3. **As per Claim 1**, AAPA teaches a method for transmitting data in a multi-chip system **[see AAPA, Paragraph 0004 – "...electronic systems having a multi-chip system frame"]**, the multi-chip system comprising at least a host chip engaged in controlling operations of the multi-chip system **[see AAPA, Paragraph 0004 – "...host chip engaged in controlling the operation of the system"]** and at least a slave chip engaged in executing servo control or signal detection **[see AAPA, Paragraph 0004, "...and at least a slave chip engaged in executing servo control or detecting some particular signals"]**.

AAPA further teaches a method of the slave chip informing the host chip of a data needed to be transmitted **[see AAPA, Paragraph 0008]**. AAPA fails to explicitly disclose a method of host chip informing the slave chip to transmit the data upon receiving the state change and further the slave chip transmitting the data to the host chip. Fujii, in an analogous art of multi-chip data transfer, teaches the above limitation including:

(a) Slave unit informing the host unit of data needs to be transmitted **[see Fujii, Col. 6, Lines 55-60, "a transfer request signal "DREQ" is outputted..."]** (This limitation was also taught by AAPA)

(b) When being informed by the slave unit, the host unit informing the slave unit to start to transmit the data **[Col. 6, Lines 55-60, "...transfer acknowledge signal DACK is sent back"]**

(c) When being informed by the host unit, slave unit starting to transmit the data to the host unit **[see Fujii, Col. 4, Lines 20-27, also see Col. 6, Lines 55-60, "...and data is written in RAM without passing through the register of microprocessor"]**

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the teachings of AAPA with that of Fujii in order to take advantage of lowering system costs with respect to data packet transmissions **[see Fujii, Col. 2, Lines 61-67]**. It is for this reason that one of

ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings above.

4. **As per Claim 3**, AAPA as modified by Fujii above teaches wherein the slave chip actively alters a voltage on a request pin pair, electrically connected between the host chip and the slave chip, to inform the host chip of the data needed to be transmitted **[see Fujii, Fig. 5, Element 'DREQ']**

5. **As per Claim 4**, AAPA as modified by Fujii above teaches a method wherein the slave chip detects states of a plurality of signals, when any changes of the states of the plurality of the signals are detected, the slave chip actively alters a voltage on a request pin pair to inform the host chip of the data needed to be transmitted, wherein the request pin pair is electrically connected between the host chip and the slave chip **[see Fujii, Col. 9, Lines 61-67]**.

6. **As per Claim 5**, AAPA as modified by Fujii above teaches a method wherein the host chip detects a voltage on a request pin pair, when the host chip detects that the voltage on the request pin pair has changed, the host chip delivers a clock signal to the slave chip via a clock pin pair, wherein the request pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Fig. 5, Element 'BUSCLOCK']**

7. **As per Claim 6**, AAPA as modified by Fujii above teaches a method wherein the host chip alters a voltage on a latch pin pair for informing the slave chip to start transmitting the data, wherein the latch pin pair is electrically connected between the host chip and the slave chip **[see Fujii, Fig. 5, Element 'DACK']**

8. **As per Claim 7**, AAPA as modified by Fujii above teaches a method wherein the slave chip transmits the data to the host chip via a data pin pair on a basis of a clock signal of a clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Col. 6, Lines 49-53]**.

9. **As per Claim 8**, AAPA as modified by Fujii above teaches a method wherein the slave chip transmits states of a plurality of signals to the host chip via a data pin pair on a basis of a clock signal of a

clock pin pair, wherein the data pin pair and the clock pin pair are both electrically connected between the host chip and the slave chip **[see Fujii, Col. 4, Lines 44-50]**.

10. **As per Claim 9**, AAPA as modified by Fujii above teaches a method wherein the method further comprises the host chip receiving data from the slave chip and decoding the data **[see Fujii, Col. 4, Line 66 – Col. 5, Line 3]**.

11. **As per Claim 10,** AAPA as modified by Fujii above teaches a method wherein the slave chip is an analog chip and the host chip is a digital chip **[see AAPA, Paragraph 0004, "...host chip is a digital chip, and the slave chip is an analog chip]**.

12. **As per Claim 11,** AAPA as modified by Fujii above teaches a method wherein the multi-chip system is an optical disk drive **[see AAPA, paragraph 0005,** *"Take an optical disk drive for example..."***]**

13. **As per Claim 12,** AAPA as modified by Fujii above teaches a method wherein the slave chip is a servo control chip and the host chip is for controlling operations of the optical disk drive **[see AAPA, paragraph 0005,** *"The task of the slave chip is to execute the servo control of the optical disk drive and detect some particular signals, such as tracking servo signal, a focusing servo signal, a trap open signal..."***].**

14. **As per Claim 22,** Combination of Claims 1, 7 and 8 teaches the limitations of Claim 22.

15. **As per Claim 23**, AAPA as modified by Fujii above teaches a method wherein when the slave chip has data needing to be transmitted to the host chip, the slave chip is asserting a voltage on the request pin pair to thereby inform the host chip of the data needing to be transmitted **[see Fujii, Col. 9, Lines 61-67].**

16. Claims 2, 13-21 and 24-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Fujii and further in view of Satoh et al, U.S. Pub No: 2003/0128702 **[herein after Satoh]**.

17. **As per Claims 2, 13, 14 and 24** AAPA and Fujii teach the limitations of Claim 1, however fail to disclose a system wherein the host chip further delivers a clock signal to the slave chip. Satoh, of

analogous art of communication methods between multi-chip systems provide a host chip **[see Satoh, Fig. 1, element 1, "Master device"]** and slave chip **[see Fig. 1, elements 3-1 – 3-n, "slave device group"]**. Furthermore, Satoh teaches a system wherein the host chip provides the slave chips with a synchronizing clock signal **[see Satoh, Paragraph 0057]**.

It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to combine the above teachings in order to provide a variable time-division multiplex communication method and apparatus in the system **[see Satoh, Paragraph 0008]**. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the above teachings.

18. **As per Claim 15,** AAPA and Fujii as modified by Satoh above teaches a method wherein when being informed by the host chip, the slave chip transmitting a fixed number of servo signals to the host chip; wherein the fixed number is equal to the predetermined number and one servo signal is transmitted by the slave chip to the host chip during each clock cycle **[see AAPA, paragraph 0006]**

19. **As per Claim 16,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a tracking servo signal **[see AAPA, paragraph 0005,** *"...tracking servo signal"***]**

20. **As per Claim 17,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a focusing servo signal **[see AAPA, paragraph 0005,** *"...focusing servo signal"***]**

21. **As per Claim 18,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a tray open signal **[see AAPA, paragraph 0005,** *"...a tray open signal"***]**

22. **As per Claim 19,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a tray close signal **[see AAPA, paragraph 0005,** *"...a tray close signal"***]**

23. **As per Claim 20,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a disk blank signal **[see AAPA, paragraph 0005,** *"...disk blank signal"***]**

24. **As per Claim 21,** AAPA and Fujii as modified by Satoh above teaches a method wherein at least one of the servo signals is a disk defect signal **[see AAPA, paragraph 0005,** *"...disk defect signal"***]**.

25. **As per Claim 25**, AAPA and Fujii as modified by Satoh above teaches a method wherein the host chip is further for de-asserting the voltage on the latch pin pair a period of time after asserting the voltage on the latch pin pair to thereby inform the slave chip to start transmitting the data **[see Fujii, Col. 9, Lines 61-67]**.

26. **As per Claim 26**, AAPA and Fujii as modified by Satoh above teaches a system wherein the slave chip is further for transmitting the data sequentially to the host chip via the data pin pair on the basis of the clock signal upon the de-assertion of the voltage on the latch pin pair **[see Fujii, Col. 4, Lines 20-27, also see Col. 6, Lines 55-60]**

27. **As per Claim 27**, AAPA and Fujii as modified by Satoh above teaches a system wherein the host chip is further for decoding the data received via the data pin pair from the slave chip on the basis of the clock signal **[see Fujii, Col. 4, Line 66 – Col. 5, Line 3].**

28. **As per Claim 28**, AAPA and Fujii as modified by Satoh above teaches a system wherein when the data has been fully transmitted from the slave chip to the host chip, the slave chip and the host chip are for holding the request pin pair, the data pin pair, the latch pin pair, and the clock pin pair at initial values while waiting for the next data transmission **[see Fujii, Col. 6, Lines 32-40]**

Conclusion

29. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JSV
12/21/07

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